Remarks/Arguments

The Final Office Action dated March 18, 2004, has been received and carefully reviewed.

Claims 1 - 8 are objected to. Appropriate correction has been made. Claims 1 - 17 stand rejected under 35 U.S.C.§112, second paragraph. Claims 1 - 17 have been amended to overcome this rejection.

Claims 1, 4, 6, 7, 9 - 11, 15, 18, 19, 21 and 22 stand rejected under 35 U.S.C. § 102 (e) as being anticipated by Bunting et al. (U.S. 5,796,743, hereinafter "Bunting"). Claims 5, 16 and 17 stand rejected under 35 U.S.C. § 103 (a) as applied to claims 1, 4, 6, 7, 9 - 11, 15, 18, 19, 21 and 22 and in further view of Takayama (U.S. 5,991,842 A, hereinafter "Takayama"). Claims 12 and 23 stand rejected under 35 U.S.C. § 103 (a) as applied to claims 1, 4, 6, 7, 9 - 11, 15, 18, 19, 21 and 22 and in further view of Sato et al. (U.S. 6,259,694 B1, hereinafter "Sato"). Claim 20 is nowhere rejected and is, therefore, assumed to be allowable. The rejections are respectfully traversed.

Independent Claim 1, as amended, recites:

> A method for assembling data packets for isochronous data transmission via a data bus, a data format for the isochronous data transmission being defined in an isochronous data format header of a bus packet, comprising the steps of:
>
> writing the isochronous data format header to a special register and to a buffer memory for the data packets when the isochronous data transmission is set up in a data transmitting device;
>
> attaching useful data of the data packet to the isochronous data format header in the buffer memory; and
>
> taking both the isochronous data format header and the useful data from said buffer memory for data transmission. (emphasis added)

The present invention is directed to a method and apparatus for assembling data packets for isochronous data transmission via a data bus. In particular, the present invention simplifies the method and circuitry for the preparation and processing of the data packets by reducing the circuitry and simplifying the method. This is accomplished by omitting as much as possible the selection logic unit (e.g., multiplexer) "for joining together the CIP header and the associated useful data". This is further accomplished by

writing the "generated CIP header ... to the buffer memory for the useful data, in which case the useful data of the data packet are subsequently attached to this CIP header in the buffer memory (see Claim 1). What is achieved as a result of this is that, for the transmission of the data via the bus, the data transmitting section only has to access the buffer memory for the useful data, where CIP header and useful data are stored contiguously in the correct order. The data transmitting section thus obtains the data to be transmitted only via the buffer memory. A selection logic unit which determines the special register from which the CIP header has to be taken and the memory area of the buffer area from which the useful data have to be attached can be omitted." (see page 3, line 32 to page 4, line 8).

Independent Claim 1 of the present invention has been amended to specifically recite "taking both the isochronous data format header and the useful data from said buffer memory for data transmission" which is supported on page 3, line 26 - page 4, line 3 and at page 11, lines 15 - 16.

In sharp contrast, Bunting describes joining data with a packet alignment flag (PAF) using a data/header combiner circuit 15, which includes a data FIFO 16 and a header FIFO 17 as depicted in Fig. 1 and more particularly in Fig. 17, which includes details of data/header combiner 15. It can be clearly seen from Fig. 17 and col. 8, lines 9 - 39 that the data/header combiner 15 of Bunting includes separate data and header FIFOs (72 and 70 respectively) and a multiplexer 76 (e.g., selection logic unit).

It is respectfully submitted that, in fact, Bunting teaches away from the present invention. As recited in independent claim 1, both the isochronous data format header and the payload (useful data) are taken from a buffer in which the packet is already formed in the right format. It is further respectfully submitted that the present invention is, therefore, not anticipated and is patentable over Bunting.

Independent claims 6, 9 and 18 have been similarly amended to recite taking/reading "both the isochronous data format and useful data from said buffer memory for data transmission".

Regarding claims 5, 16 and 17, Takiyama describes the format of a CIP packet and that a source packet may be divided in a number of data blocks, but is silent to how

the CIP packet is formed in memory. In particular, Takiyama does not describe the use of a single buffer (or FIFO) for assembling data or simplification of the method and circuitry required for assembling data packets by omitting a selection logic unit from the combiner circuitry.

Regarding claims 12 and 23, Sato describes in detail the isochronous cycle of a IEEE1394 bus inclusive of the isochronous bus packet format and the late check (error bit). Sato also describes at col. 10, line 35 to 40 that the post-transmission circuit 107 adds the 1394 header and CIP header to the data containing a source packet header stored in the FIFO. Data flow in Fig. 5 is from FIFO 110 to Link Core 101 via post processing unit 107. The CIP header is added to the source packet 'On the Fly'. This teaches away from the present invention in which both the CIP header and the source packet data is taken/read from the buffer memory.

It is respectfully submitted that Bunting alone or in combination with either Takiyama or Sato does not include all of the features of the present invention. In light of the above remarks, it is respectfully submitted that independent claims 1, 6, 9, and 18, for at least the reasons stated above, are unanticipated and patentable over the art of record. Claims 2 - 5 depend directly or indirectly from claim 1. Claims 7 - 8 depend directly from claim 6. Claims 10 - 17 depend directly or indirectly from claim 9. Claims 19 - 23 depend directly from claim 18. It is, therefore, respectfully submitted that claims 2 - 5, 7 - 8, 10 - 17 and 19 - 23 are also unanticipated and patentable for at least the reasons discussed above as well as the additional features recited therein.

New independent clams 24 - 27 have been added. These claims are directed to inclusion of a comparison value in the isochronous data format header, wherein the comparison value is a data block count. None of the art of record describes this feature. It is, therefore, respectfully submitted that the newly added claims 24 - 27 are also unanticipated and patentable over the art of record.

If you have any questions regarding this response, please do not hesitate to contact me.

Please charge the $800 fee for the 4 newly added independent claims, and any other costs that may be associated with the filing of this response, to Deposit Account No. 07-0832.

Respectfully submitted,
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